7. (Amended) A method of manufacturing a semiconductor device with a semiconductor element fixed to a semiconductor package, comprising the steps of:

preparing said semiconductor package structured by providing a substrate for mounting said semiconductor element thereon to fix said semiconductor element to one side thereof and a connecting pattern provided on the other side of said substrate and by forming a through hole from the one side to the other side of said substrate;

fixing a surface where the element is formed of said semiconductor element on the one side of said substrate of said semiconductor package such that an electrode of said semiconductor element is within said through hole;

electrically connecting said connecting pattern and said electrode of said semiconductor element via wires through said through hole; and

sealing said through hall and said wires with resin.

8. (Amended) A method of manufacturing a semiconductor device as claimed in claim 7, wherein said connecting pattern is provided continuously in a plurality of stages and an end portion of said connecting pattern on the side of said through hole is provided on a stage on the side ~~of the one said~~ of said substrate.

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9. (Amended) A method of manufacturing a semiconductor device as claimed in claim 7, wherein said through hole is a plurality of through holes.

Kindly add the following new Claims 24-27:

24. (New) A method of manufacturing a semiconductor device, comprising:

providing a substrate having a first surface and a second surface opposed to the first surface, and further having an elongate opening defined therethrough from the first surface to the second surface;

forming a plurality of connecting patterns on the second surface of said substrate, each of the plurality of connecting patterns having a first end;

mounting a surface of a semiconductor chip to the first surface of the substrate, wherein a plurality of electrodes are located on the surface of said semiconductor chip and wherein the surface of the semiconductor chip is mounted to the first surface of the substrate such that the plurality of electrodes are aligned over said elongate opening of said substrate;

respectively electrically connecting said plurality of electrodes to corresponding ones of said plurality of patterns by a plurality of wires extending within the elongate opening of said substrate; and

covering said plurality of electrodes, said plurality of wires, and the first ends of said plurality of connecting patterns with a resin.

25. (New) The method as claimed in claim ~~16~~, wherein said substrate is provided so as to include an upper plate and a lower plate which define a step configuration in the second surface of said substrate, wherein the upper plate is located between said semiconductor chip and said lower plate, and wherein the plurality of connecting patterns are formed so as to extend continuously from said upper plate to said lower plate such that the first end of the plurality of connecting patterns are located on said upper plate.

26. (New) A method of manufacturing a semiconductor device, comprising:

providing a substrate having a first surface and a second surface opposed to the first surface, and further having at least first and second elongate openings defined therethrough from the first surface to the second surface;

forming a plurality of connecting patterns on the second surface of said substrate, each of the plurality of connecting patterns having a first end;

mounting a surface of a semiconductor chip to the first surface of the substrate, wherein a plurality of electrodes are located on the surface of said

semiconductor chip and wherein the surface of the semiconductor chip is mounted to the first surface of the substrate such that each of the plurality of electrodes is aligned over one of said first and second elongate openings of said substrate;

respectively electrically connecting said plurality of electrodes to corresponding ones of said plurality of patterns by a plurality of wires extending within the first and second elongate openings of said substrate; and

covering said plurality of electrodes, said plurality of wires, and the first ends of said plurality of connecting patterns with a resin.

27. (New) A method as claimed in claim 26, wherein said substrate is provided so as to include an upper plate and a lower plate which define a step configuration in the second surface of said substrate, wherein the upper plate is located between said semiconductor chip and said lower plate, and wherein the plurality of connecting patterns are formed so as to extend continuously from said upper plate to said lower plate such that the first end of the plurality of connecting patterns are located on said upper plate.